MJD200 (NPN)
MJD210 (PNP)

Complementary Plastic Power Transistors

NPN/PNP Silicon DPAK For Surface Mount Applications

Designed for low voltage, low−power, high−gain audio amplifier applications.

Features

- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain − h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2 Adc
  = 10 (Min) @ I_C = 5 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current−Gain − Bandwidth Product −
  f_T = 65 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage −
  I_{CBO} = 100 nAdc @ Rated V_{CB}
- Epoxy Meets UL 94, V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V
- Pb−Free Packages are Available

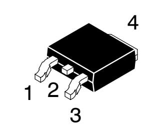


ON Semiconductor®

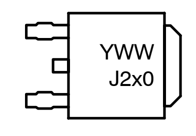
http://onsemi.com

SILICON
POWER TRANSISTORS
5 AMPERES
25 VOLTS
12.5 WATTS

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



Y = Year
WW = Work Week
x = 1 or 0

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

February, 2005 − Rev. 6
Publication Order Number:
MJD200/D

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Base Voltage	V_{CB}	40	Vdc
Collector−Emitter Voltage	V_{CEO}	25	Vdc
Emitter−Base Voltage	V_{EB}	8	Vdc
Collector Current − Continuous Peak	I_C	5 10	Adc
Base Current	I_B	1	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.4 0.011	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	10	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	89.3	°C/W

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 1), (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	−	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	 − −	 100 100	 nAdc μAdc
Emitter Cutoff Current (V_{BE} = 8 Vdc, I_C = 0)	I_{EBO}	−	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (Note 1), (I_C = 500 mAdc, V_{CE} = 1 Vdc) (I_C = 2 Adc, V_{CE} = 1 Vdc) (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	 70 45 10	 − 180 −	−
Collector−Emitter Saturation Voltage (Note 1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2 Adc, I_B = 200 mAdc) (I_C = 5 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	 − − −	 0.3 0.75 1.8	Vdc
Base−Emitter Saturation Voltage (Note 1), (I_C = 5 Adc, I_B = 1 Adc)	$V_{BE(sat)}$	−	2.5	Vdc
Base−Emitter On Voltage (Note 1), (I_C = 2 Adc, V_{CE} = 1 Vdc)	$V_{BE(on)}$	−	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (Note 2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	−	MHz
Output Capacitance MJD200 (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD210	C_{ob}	− −	80 120	pF

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

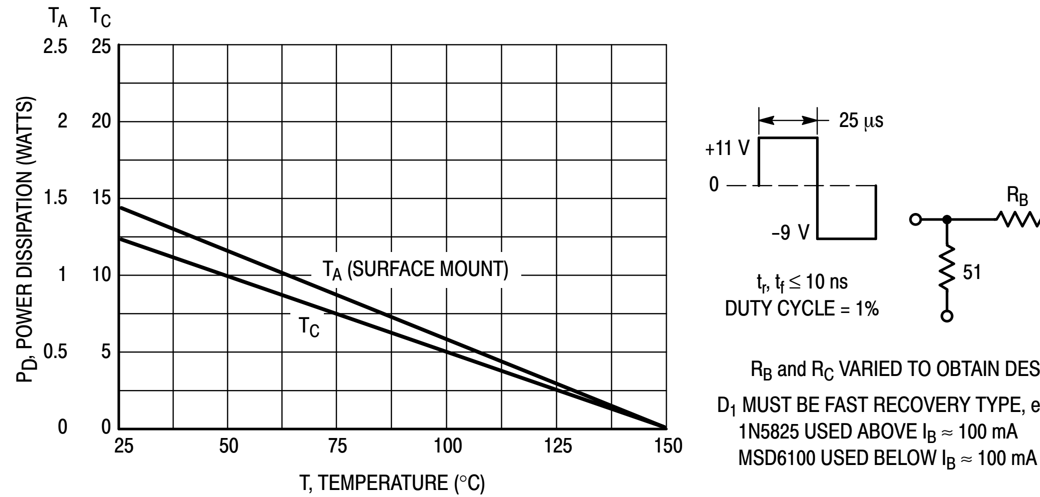


Figure 1. Power Derating

Figure 2. Switching Time Test Circuit

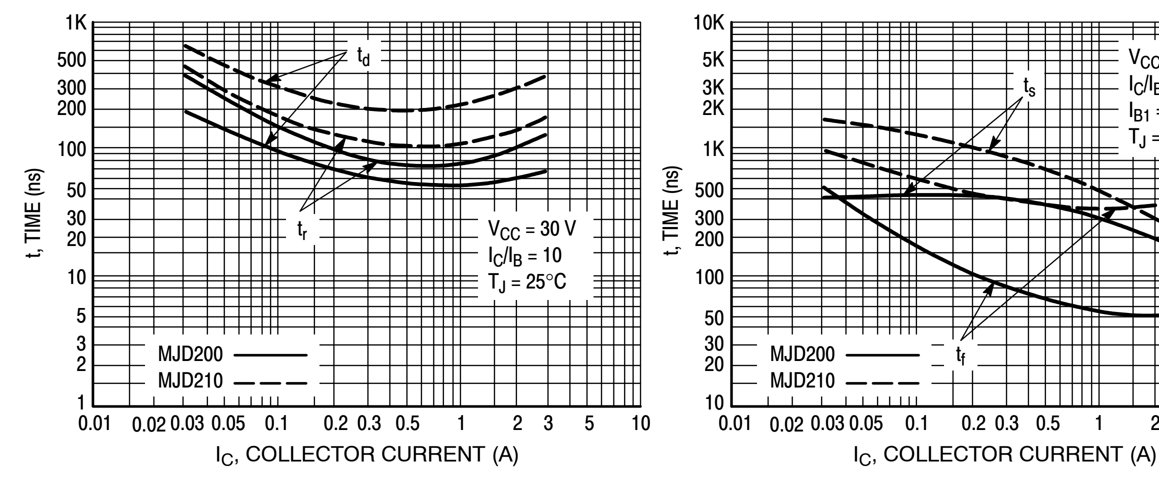


Figure 3. Turn−On Time

Figure 4. Turn−Off Time

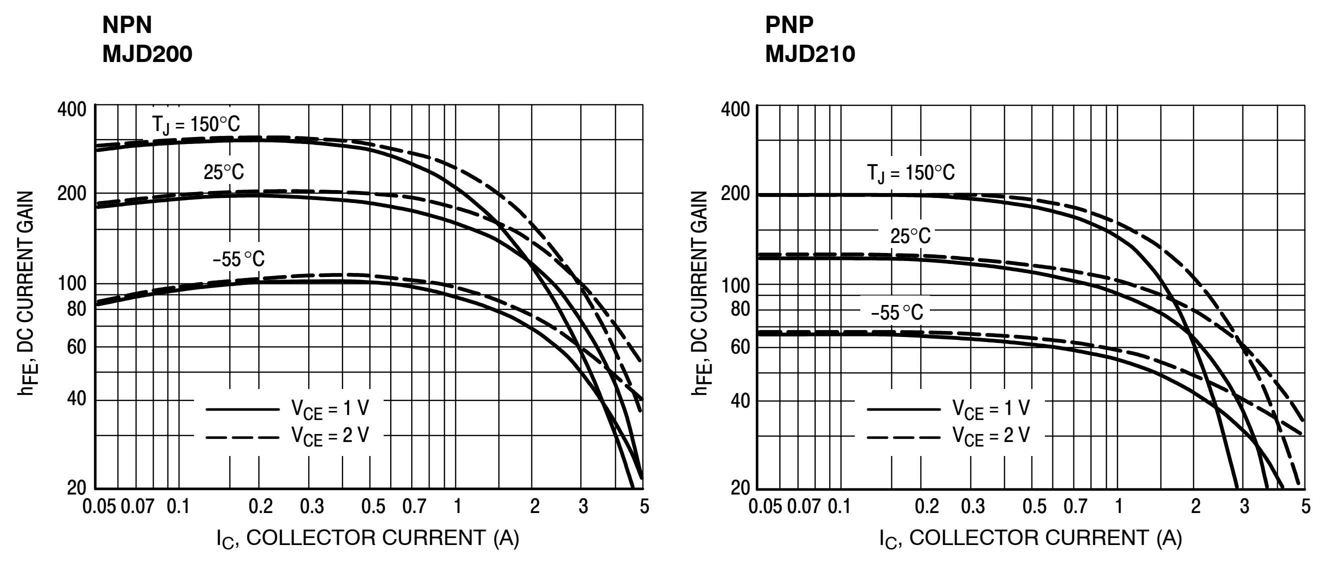


Figure 5. DC Current Gain

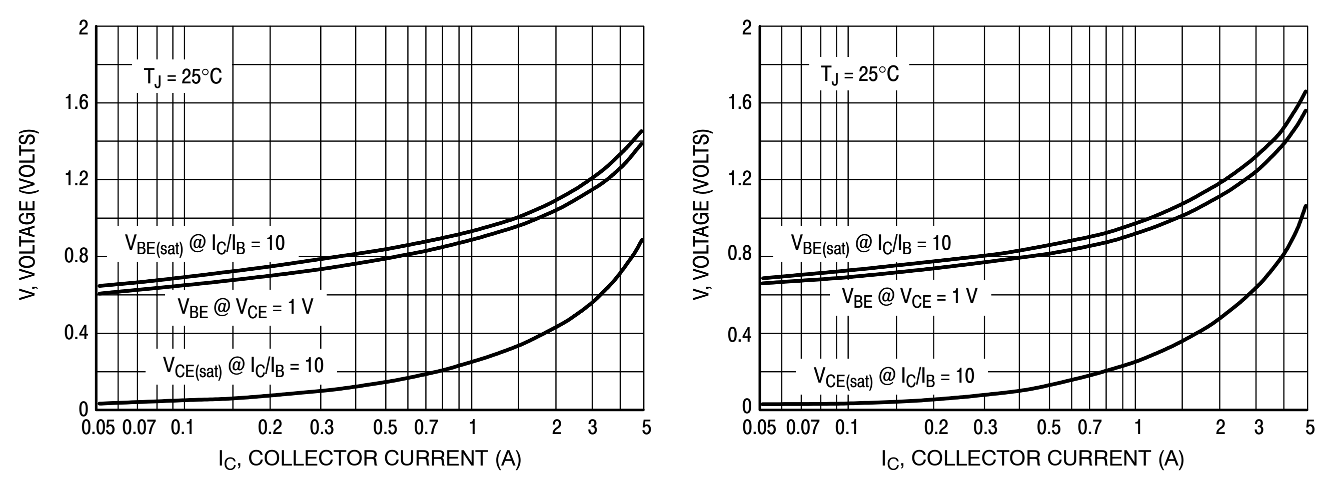


Figure 6. “On” Voltage

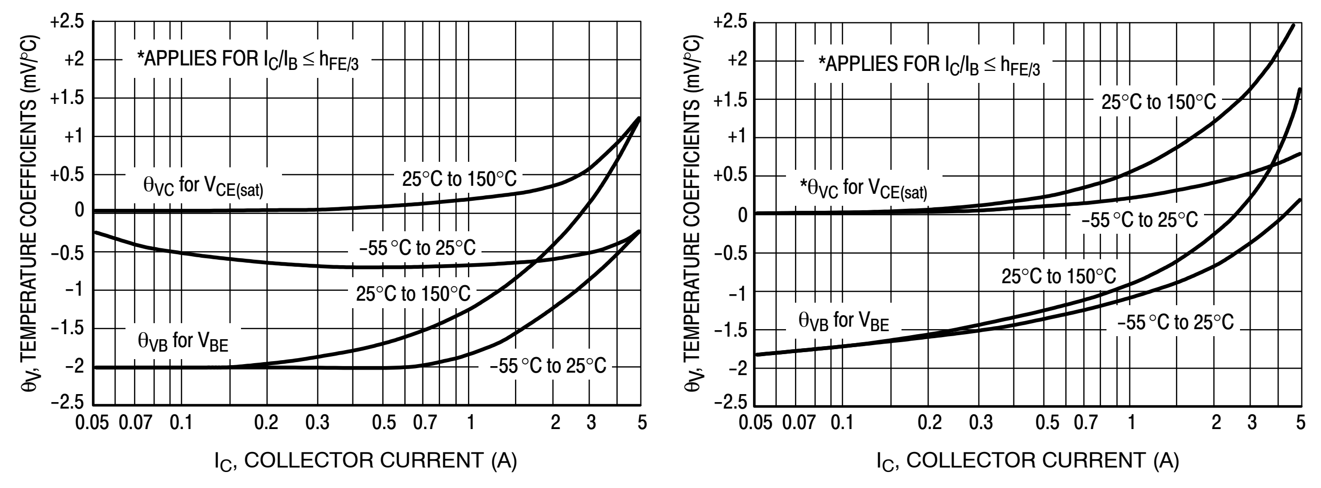


Figure 7. Temperature Coefficients

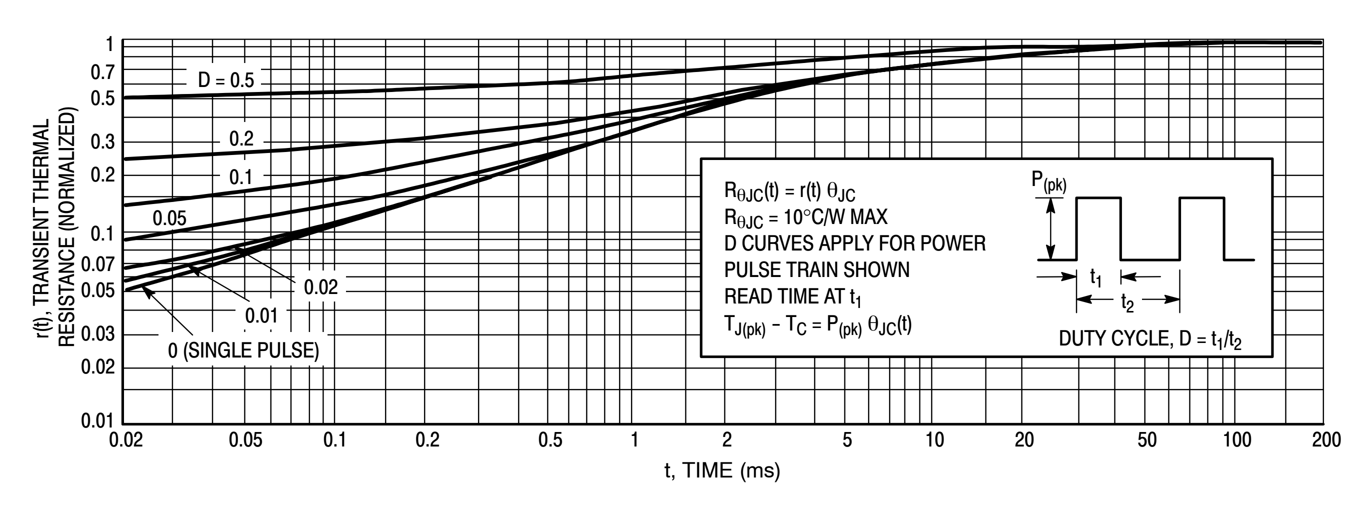


Figure 8. Thermal Response

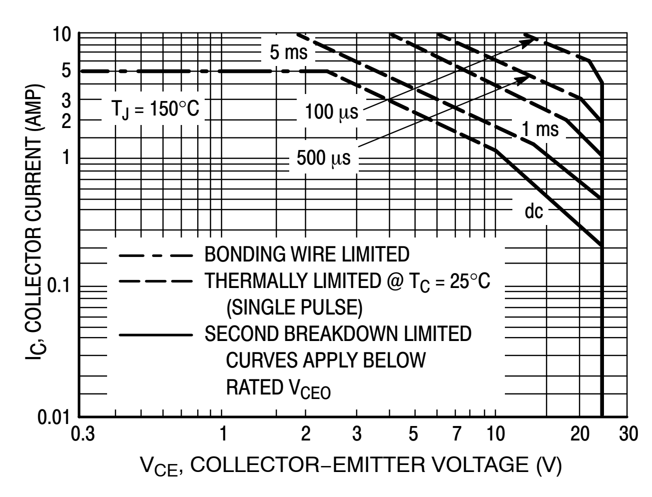


Figure 9. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

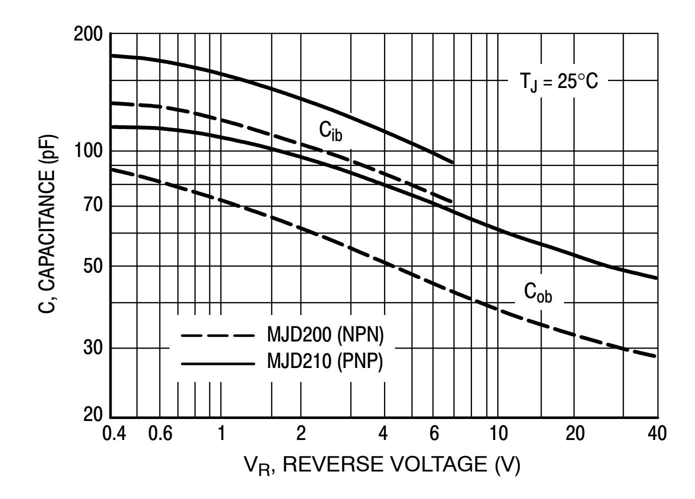


Figure 10. Capacitance

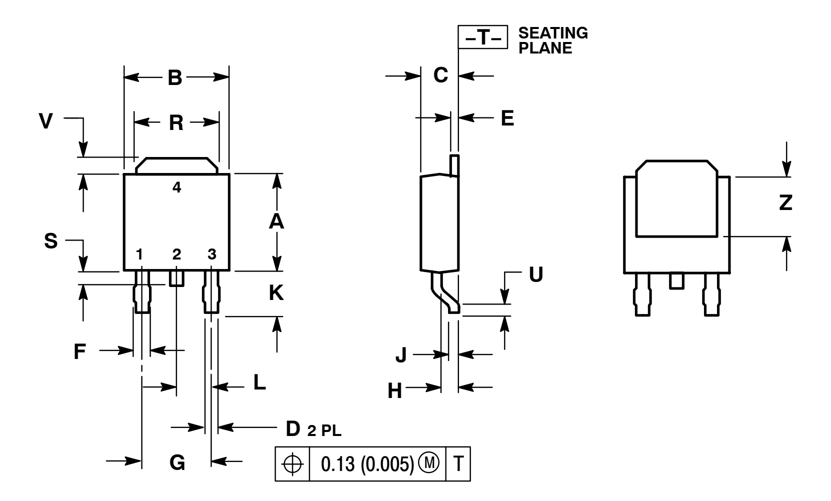
ORDERING INFORMATION

Device	Package Type	Shipping†
MJD200	DPAK	75 Units / Rail
MJD200G	DPAK (Pb−Free)	75 Units / Rail
MJD200RL	DPAK	1800 Tape & Reel
MJD200RLG	DPAK (Pb−Free)	1800 Tape & Reel
MJD200T4	DPAK	2500 Tape & Reel
MJD200T4G	DPAK (Pb−Free)	2500 Tape & Reel
MJD210	DPAK	75 Units / Rail
MJD210RL	DPAK	1800 Tape & Reel
MJD210T4	DPAK	2500 Tape & Reel
MJD210T4G	DPAK (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE O

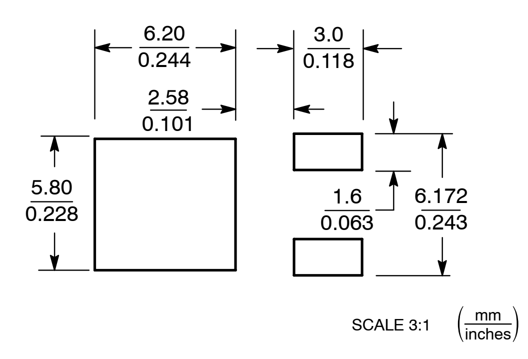


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.